**Flip Chip Interconnect**

***Course Leader: Eric Perfecto – IBM Research***

**Course Objective:**

This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various type of wafer bumping technologies, solder joint formation, non-solder joints and assembly considerations. The course is divided into two sections. The first section focuses on the key steps of flip chip assembly technologies and their associated equipment and materials. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today’s flip chip assembly. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, etc. Special focus of the course will be on fine pitch technologies, mainly u-Pillar and Hybrid bonding.

**Course Outline:**

1. Introduction to Flip Chip Technologies

2. Flip Chip Technologies: Mass Reflow vs Thermal Compression Bonding

3. Packaging Technologies

4. Bumping Ground Rules

5. Flip Chip Under-Bump Metal and Intermetallic

6. Flip Chip Solder Deposition Processes

7. Cu Pillar Technology

8. Hybrid Bonding

**Who Should Attend:**

The goal of this course is to provide the students with a comprehensive understanding of flip chip fabrication and its use on the various advanced packages. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions.

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**Eric Perfecto** has over 40 years of experience working in the development and implementation of C4 and advanced Si packages at IBM and GoblalFoundries. Eric’s responsibilities include UBM and Pb-free solder definition for C4 and u-Pillar interconnect, and yield improvements in C4 and 3D wafer finishing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College. Eric has published over 80 external papers, including two best Conference Paper Awards and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds 60 US patents and has been honored with three IBM Outstanding Technical Awards. Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. Eric is an IEEE Fellow, an EPS Distinguish Lecturer and EPS VP of Education.